BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

REMARKS

Claims 1-8 remain active in this application. Claims 9-17 have previously been canceled. The specification has been reviewed and editorial revisions made where seen to be appropriate. Claims 5, 7, and 8 have been editorially revised. Claim 1 has been amended to provide definition with the claim of the term "sub-lithographic" based on a definition of "sub-lithographic" which is well-known in the art. Support for the amendment to claim 1 is found throughout the specification particularly in Figure 2 and paragraphs 0010 and 0023. No new matter has been introduced into the application.

The Examiner has required additional illustration in regard to the spatial positioning of the source and drain regions and damascene connections. In response, approval has been requested for revisions of the drawings based on the requirement stated by the Examiner as shown in the attached drawing sheets. (These sheets also alter scale and orientation of some Figures to correspond to other Figures and to add reference numerals in an effort to facilitate the Examiner's understanding of the depictions of the invention therein.) Sidewall 32 has also been added as described in paragraph 0027 and such a depiction was approved in the parent application. Additionally, a further sheet containing a figure designated, for convenience, as Figure 5B, is attached to show a cross-sectional view orthogonal to Figure 5A and extending in the channel region. It is respectfully submitted that Figure 5B is not necessary to an understanding of the invention or complete illustration of the claimed subject matter but addition of such a Figure is acceptable to Applicants, should the Examiner so require. Reference numeral 42 has been added in Figures 3A, 3AB, 4A, and 5A, to further emphasize the

spatial positioning of the source and drain locations in accordance with the specification, specifically in paragraph 0019, lines 5-6, and the above revised paragraph 0025, lines 7-12, and paragraph 0028, line 9. The positioning of the source and drain regions are further emphasized in Figure 5B. In view of these revisions, all rejections based on incomplete illustration of the spatial positioning of the source/drain regions are respectfully traversed and approval of the proposed drawing revisions and reconsideration and withdrawal of this objection are respectfully requested.

In regard to the damascene connections, it is respectfully submitted that such terminology is well-understood in the art to refer to conductors formed such as to be supported laterally by material, for example, by removing material and filling the space so created with conductive material, precisely as stated in regard to removal of nitride to connect the gates, if desired, as noted in paragraph 0030. The term derives from a technique in which a groove or recess in a surface is filled by providing a layer of material which is then patterned by removal of the layer (e.g. by polishing) to the original surface leaving the material in the groove. This structure and technique are well-described in paragraphs 0030 and 0031. Such a structure is well illustrated in Figures 5, 5A, and 5B where connection 50, which may be a damascene connection, is formed below the surface of the nitride and the outline of the recesses for source, drain and gate connections are clearly shown. As identified by reference numerals 50 and 50', the connection to the gate (and/or source and drain) may be made to the silicide sidewall or liner or to the gate, source and/or drain polysilicon directly and may or may mot include a damascene portion 50'. However, the placement of the third connection, which may be a

damascene connection, is further emphasized in the addition of Figure 5B in cross-section BB' in accordance with the drawing corrections required by the Examiner. In view of these revisions and the emphasis thereof, all rejections by the Examiner based on illustration of the damascene connections are believed to be fully answered.

Claims 4, 5, 7 and 8 have been rejected under 35 U.S.C. §112, first paragraph, as being drawn to subject matter which is not supported by enabling disclosure in regard to damascene connections. This ground of rejection is respectfully traversed.

As discussed above in connection with the drawings, damascene connections are well-known and well-understood in the art. Damascene connections are formed by "by lithographically defining and etching openings in the STI material at appropriate locations and depositing metal in the openings and on the surface as shown at 50 of Figure 5", as explicitly recited in paragraph 0030. This summary of the damascene process is entirely sufficient to enable damascene connections to be made without undue experimentation by those skilled in the art and who would be familiar with damascene connection structures for that reason even if damascene connections and the process for making them were not well-known and well-understood in the art. Since damascene connections are, in fact, well-known and well-understood in the art, even this description of the technique of their formation is unnecessary to enablement of the successful practice of the invention by persons skilled in the art. Therefore, it is respectfully submitted that this ground of rejection is clearly in error and reconsideration and withdrawal of the same is respectfully requested.

Claims 1 - 3 have been rejected under 35 U.S.C. §103 as being unpatentable over Mizuno et al. in view of Sung and claims 4 - 8 have been rejected under 35

U.S.C. §103 as being unpatentable over Mizuno et al. in view of Sung and Liu et al. These grounds of rejection are respectfully traversed for the reasons of record which are hereby fully incorporated by reference and the further reasons set out below.

Mizuno et al. is directed to formation of a transistor at small size and improving the turn-off characteristics thereof and thus superficially resembles the invention in several respects such as formation of a gate structure which partially surrounds the conduction channel (a structural feature indicated to be known, but having potential disadvantages avoidable by the present invention) and having recessed gate regions positioned on opposing sides of the conduction channel. However, Mizuno et al. does not teach or suggest formation of the conduction channel to have a sub-lithographic width as now explicitly defined in the claims (e.g. of dimensions similar to those described at paragraph 0006 of the present application) preferably achieved by undercutting of a mask as illustrated in Figure 2 (which supports the particularly improved turn-off characteristics of the transistor in accordance with the invention since the distance over which the gate must control the conduction of the channel is reduced as well as the sub-lithnographic nature and dimensions of the channel structure - the channel of Mizuno et al. is clearly defined lithographically and thus cannot be sub-lithographic), a gate structure which is recessed from the source and drain regions (which supports the reduction of gate capacitance as noted in paragraph 0028 - Mizuno et al. forms source and drain regions in a "self-matched" (e.g. self-aligned) manner using the gate as a mask as noted at column 8, lines 15 - 32 such that the gate is contiguous with the source and drain regions), or silicide sidewalls on the source drain *and* gate (which supports reduction of resistance of these

elements). Particularly in combination, these features of the invention provide further improvement in performance and electrical characteristics while being capable of manufacture at smaller size than the transistor of Mizuno et al. Only the last of these three clear deficiencies of Mizuno et al. is recognized by the Examiner.

These deficiencies of Mizuno et al. to answer the claimed subject matter are not remedied or even mitigated by Sung and/or Liu et al. Sung is cited by the Examiner for teaching silicide spacers 8. However, column 3, lines 56 and 60 clearly identify these spacers as being tungsten and the description of their formation does not suggest silicidation. Liu et al. is cited for teaching formation of damascene interconnects which is correct but does not teach or suggest any other of the claimed features noted above which are not taught or suggested by Mizuno et al. Since the statements of the rejections are silent as to the features of sub-lithographic channel width and recessing of the transistor gate from the source and drain and incorrect in regard to the provision of silicide, especially on all of the gate, source and drain regions of the transistor, the Examiner has failed to make a *prima facie* demonstration of obviousness of any claim in the application. By the same token, the references do not provide evidence of a level of ordinary skill in the art which would support the conclusion of obviousness that the Examiner has asserted, particularly since they do not lead to an expectation of success in deriving the meritorious effects of the invention such as further improved electrical characteristics at smaller sizes.

Further, the Examiner maintains that the term "sub-lithographic" is not an appropriate device limitation. However, it is respectfully submitted that the term "sub-lithographic" is a well-recognized term

of art connoting that the dimension referenced is not directly determined by lithographic patterning of a mask or resist and that the dimension is smaller than can be resolved by a lithographic exposure using a given tool or design rules (e.g. minimum feature size regime) as emphasized for clarity in the amendment to claim 1. Specifically, improvements in lithographic resolution allow scaling of devices to smaller sizes and some features of integrated circuit elements are defined as to size and location by lithographic exposure. Therefore, "sub-lithographic" is clearly an apt expression to convey a relative dimension as well as being a well-recognized and well-understood term of art. This relativity of dimensions of structure is reflected in paragraph 0006 of the present application which indicates that for short gate lengths, the gate length must be held to about two to four times the diffusion thickness; noting that it logically follows that for short gate lengths (e.g. approaching or at the minimum resolvable lithographic feature dimension) the channel width must be held to a fraction of the gate length and thus substantially smaller than the lithographically resolvable feature dimension, even though that dimension has been and presumably will continue to be reduced. *Therefore, it is respectfully submitted that the term "sub-lithographic" is not, in fact, subject to being interpreted in various ways and that no ambiguity or lack of clarity as to claim scope or impediment to determination thereof is presented by use of the term and reconsideration and withdrawal of this ground of rejection is respectfully requested.* Further, the stated grounds of rejection are clearly in error in failing to consider express recitations of the claims such as those noted above as well as failing to determine the level of ordinary skill in the art (e.g. the teaching of damascene connections in Liu et al. clearly indicates the impropriety of the rejections

under 35U.S.C. §112, first paragraph, or recognition of the well-understood term "sub-lithographic"). Rather, the Examiner has used clearly improper rejections under 35 U.S.C. §112 to buttress rejections based on prior art which do not answer the express recitations of the claims.

Accordingly, it is respectfully submitted that the stated grounds of rejection are in error and untenable, particularly as the claims have been further clarified by amendment. Therefore, reconsideration and withdrawal of the rejections based on prior art is respectfully requested.

By the same token it is respectfully submitted that the finality of the present office action is premature. An action may not properly be made final when a *prima facie* demonstration of the propriety of the rejections contained therein has not been made. Therefore it is respectfully requested that the finality of the action be withdrawn and the above-requested amendments made as a matter of right. In any case, it is also respectfully submitted that entry of the above-requested amendments is well justified and in order. The amendments do not raise new issues since the amendments are directed to emphasizing structure recited in the claims as finally rejected. The requested amendments are also well-justified as placing the application in condition for allowance or, in the alternative, better form for Appeal by reducing and/or simplifying issues. Accordingly, entry of the requested amendments is respectfully requested.

Since all rejections, objections and requirements contained in the outstanding official action have been fully answered and shown to be in error and/or inapplicable to the present claims, it is respectfully submitted that reconsideration is now in order under the provisions of 37 C.F.R. §1.111(b) and such reconsideration is respectfully requested. Upon

reconsideration, it is also respectfully submitted that this application is in condition for allowance and such action is therefore respectfully requested.

If an extension of time is required for this response to be considered as being timely filed, a conditional petition is hereby made for such extension of time. Please charge any deficiencies in fees and credit any overpayment of fees to Deposit Account No. 09-0458 of International Business Machines Corporation (East Fishkill).

Respectfully submitted,

Marshall M. Curtis
Reg. No. 33,138

Whitham, Curtis & Christofferson, P. C.
11491 Sunset Hills Road, Suite 340
Reston, Virginia 20190

Customer Number: **30743**
(703) 787-9400

Attachments:
- Copy of Figure 5 of informal drawings from parent application
- Six sheets of proposed drawing revisions
- Additional Sectional view of Figure 5, designated Figure 5B